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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,489	04/28/2005	Torayuki Tsukada	10921.313USWO	4098

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,489	TSUKADA ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *20-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-19 in the reply filed on 28 December 2006 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **1-3, 5 and 7** are rejected under 35 U.S.C. 102(b) as being anticipated by May (US 4,706,060).

4. Regarding claims **1-3, 5 and 7**, May discloses in Fig 6 and Fig 7 a chip resistor comprising a chip-form resistor having a front surface (top) and a rear surface (bottom) provided at an interval in a thickness direction and a pair of side faces (511A and 513A) extending in a fixed direction at an interval in a width direction, and a plurality of electrodes (two items, 518, 520) provided in series on the rear surface of the resistor at intervals in the fixed direction and also removed from edges of the rear surface in the fixed direction (Fig 6, item 518 and 520 are raised by items 540 and 542), wherein the

chip resistor also comprising: a first insulation layer (Fig 4 item 330, glass) covering regions between the plurality of electrodes on the front surface and the rear surface of the resistor; and a second insulation layer (540A, 542A) covering the pair of side faces of the resistor.

5. Claims **18 and 19** are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi (US 6,955,942).

6. Regarding claims **18 and 19**, Kobayashi discloses in Fig 6B a frame constituted by a conductive member (60) comprising a plurality of plate-form portions (50) extending in a fixed direction, each plate-form portion having a front surface, a rear surface, and a pair of side faces (Fig 6C cross section), and a support portion for supporting the plurality of plate-form portions (outside strips with holes 100), wherein a connecting portion (see Fig 6B) between each of the plate-form portions and the support portion is formed narrower than the plate-form portion and wherein the support portion has a frame shape, and each of two end portions in a length direction of each of the plate-form portions is supported on the support portion via the connecting portion (see Fig 6B).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over May and Sato (US 6,777,778). May discloses the resistor of claim 2, but does not specify that the thickness of each of the electrodes is greater than the thickness of the first insulation layer.

Sato teaches that the electrode thickness of chip resistors should be as great as possible, and as seen in Fig 1, thicker (5) than the first insulation layer (2) in order to reduce the resistance of the electrodes and increase the accuracy of the resistance (col 2 ln 18-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Sato on the resistor of May in order to increase the accuracy of the resistor.

10. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over May and Gardner (US 5,170,146). May discloses the resistor of claim 1, but does not specify

wherein a pair of end faces are provided at intervals with a solder layer formed on each of the end faces.

Gardner teaches that most chip resistors have a metal base coating covered with a nickel barrier layer and a top solder layer in order to assure a reliable electrical connection to a circuit board while preventing leaching of the base coat (col 1 ln 40-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Gardner in the resistor of May in order to ensure a reliable electrical connection..

11. Claims **8 and 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Caporali (EP 0 326 212) and May. Caporali discloses in Fig 1 a manufacturing method for a chip resistor, comprising the steps of: producing a bar-form resistor aggregate (Fig 1D) in which a plurality of electrodes (3) is provided on a rear surface of a bar-form resistor material, the plurality of electrodes being arranged at intervals in a length direction of the resistor material, and regions between the plurality of electrodes on the front and rear surface are covered with first and third insulation layers (2); and dividing the resistor aggregate into a plurality of chip resistors (Fig 1E) having protruding resistor side faces (Fig 1D item 1 exposed) by cutting the resistor aggregate in a plurality of locations in a length direction thereof. Caporali does not specify forming a second insulation layer covering the pair of side faces of the resistor material.

May teaches that the side faces of chip-form resistors are covered with second insulation layers in order to fully insulate the resistor and electrodes from the environment (col 8 ln 32-41). It would have been obvious to one of ordinary skill in the

art at the time of the invention to use the teachings of May in the method of Caporali in order to fully insulate the resistor and electrodes from the environment.

12. Claims **9 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Caporali and May as applied to claim 8 above, and further in view of Doi (US 5,450,055). Caporali and May teach the method of claim 8, wherein an insulation layer is formed on the pair of side faces of the bar-form resistor material, but do not specify providing a pattern-formed insulation layer and a conductive layer serving as the electrode on one surface of a plate serving as resistor material, and then dividing the plate into the bar-form resistor material.

Doi teaches a method of manufacturing chip resistors where a patterned insulated substrate has an electrode layer and a resistor layer formed thereon, and is then divided into bar-form resistor material (col 2 ln 30-44). The process is used because it allows formation of accurate chip resistors in a smooth supply tube for automatic mounting (col 1 ln 67- col 2 ln 9). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Doi in the method of Caporali and May in order to form accurate resistors for automatic mounting.

13. Claims **13-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Caporali, May and Kobayashi.

14. Caporali discloses in Fig 1 a manufacturing method for a chip resistor, comprising the steps of: producing a bar-form resistor aggregate (Fig 1D) in which a plurality of electrodes (3) is provided on a rear surface of a bar-form resistor material, the plurality of electrodes being arranged at intervals in a length direction of the resistor

material and being formed by a plating process after formation of the insulator layers (col 2 ln 1-3), and regions between the plurality of electrodes on the front and rear surface are covered with first and third insulation layers (2); and dividing the resistor aggregate into a plurality of chip resistors (Fig 1E) having protruding resistor side faces (Fig 1D item 1 exposed) by cutting the resistor aggregate in a plurality of locations in a length direction thereof. Caporali does not specify forming a second insulation layer covering the pair of side faces of the resistor material.

May teaches that the side faces of chip-form resistors are covered with second insulation layers in order to fully insulate the resistor and electrodes from the environment (col 8 ln 32-41). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of May in the method of Caporali in order to fully insulate the resistor and electrodes from the environment. Caporali and May do not specify preparing a conductive frame with plate-form portion on which the resistors are formed, or that the frame is rotated to form the second insulator layer.

Kobayashi teaches in Fig 6B a frame for chip resistors, serving as a starting material with supporting functions (col 3 ln 22-25) constituted by a conductive member comprising a plurality of plate-form portions extending in a fixed direction, each plate-form portion having a front surface, a rear surface, and a pair of side faces, and a support portion for supporting the plurality of plate-forms, wherein a connecting portion between each of the plate-form portions and the support portion is formed narrower than the plate-form portion and wherein the support portion has a frame shape, and each of two end portions in a length direction of each of the plate-form portions is

supported on the support portion via the connecting portion. Kobayashi also teaches that it is well known in the art to rotate the frame during processing in order to work on each orthogonal angle (col 13 ln 10-20). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Kobayashi in the method of Caporali and May in order to have a starting material that could also provide support for the chip resistors.

Double Patenting

15. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

16. Claims **1-3 and 5-6** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 7,129,814. Although the conflicting claims are not identical, they are not patentably distinct from each other because the '814 patent claims a chip resistor with two insulator layers of

like materials covering the top and bottom between the electrodes, and a third insulator layer covering the side faces.

17. Claims **1-6** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 8-15 of copending Application No. 10/517,943. Although the conflicting claims are not identical, they are not patentably distinct from each other because the '943 application claims a chip resistor with two insulator layers on upper and lower surfaces (between the electrodes), a third insulator layer on the sides, and a thicker electrode.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

18. Claims **1-6 and 8-13** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7 and 8-14 of copending Application No. 10/553,044. Although the conflicting claims are not identical, they are not patentably distinct from each other because the '044 application claims a chip resistor and method of manufacture that includes two insulator layers on upper and lower surfaces (between the electrodes), a third insulator layer on the sides, and a thicker electrode.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

19. Claims **8-10, 12-13 and 15-17** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 5 and 16-20 of copending Application No. 10/517,943. Although the conflicting claims are

not identical, they are not patentably distinct from each other because the '943 application claims a manufacturing method for a chip resistor where a lead frame or metal plate is used to produce a bar-form resistor, metal plating layers are provided as connection terminals, insulator layers are provided to cover the surfaces, the plate is divided into individual resistor elements, and the connecting portion of the frame is formed narrower than the plate portion.

This is a provisional obviousness-type double patenting rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham
Examiner
Art Unit 2814

jci

HOWARD WEISS
PRIMARY EXAMINER